

CLAIMS

I Claim:

1 1. A device for combining a plurality of arithmetic flags, comprising:
2 a combination function module that examines a plurality of arithmetic flags,
3 determines field size of the plurality of arithmetic flags and based on the
4 determination of the field size will combine the plurality of arithmetic flags into a
5 single combined arithmetic flag variable, wherein the plurality of arithmetic flags
6 represent the status of a plurality of data items after a mathematical operation is
7 performed by the processor on the plurality of data items.

1 2. The device recited in claim 1, further comprising:
2 a condition check module that determines the status of the combined
3 arithmetic flag variable and causes the processor to execute an appropriate
4 operation based on the status.

1 3. The device recited in claim 1, wherein the field size is based either a
2 nibble, byte, half word, or word in length.

1 4. The device recited in claim 3, wherein the plurality of arithmetic flags
2 further comprise:
3 a negative data value, a zero data value, a carry out occurrence in a data
4 value, or an overflow condition in a data item in the plurality of data items.

1 5. The device recited in claim 4, the combination function module performs
2 either an AND or an OR operation.

1 6. The device recited in claim 2, wherein the status determined by the
2 condition further comprises:

- 3 any data item has overflowed;
4 any data item has not overflowed;
5 any data item is positive or zero;
6 any data item is negative;
7 any data item is zero;
8 any data item is not zero;
9 any data item has a carry out;
10 any data item does not have a carry out;
11 all data items have overflowed;
12 all data items have not overflowed;
13 all data items are positive or zero;
14 all data items are negative;
15 all data items are zero;
16 all data items are not zero;
17 all data items have a carry out; and
18 all data items do not have a carry out.

1 7. A method of combining a plurality of arithmetic flags for presentation to
2 a processor, comprising:

3 determining a field size of the plurality of arithmetic flags on which to base a
4 combination process, wherein the plurality of arithmetic flags represent the status of
5 a plurality of data items after a mathematical operation is performed by the
6 processor on the plurality of data items;

7 extracting the plurality of arithmetic flags based on the field size;

8 combining the plurality of arithmetic flags based on a function selected when
9 a combination process is selected; and

10 storing a result of the combining of the plurality of arithmetic flags in a
11 destination register for access by the processor.

1 8. The method recited in claim 7, wherein the field size is based either a
2 nibble, byte, half word, or word in length.

1 9. The method recited in claim 8, wherein the plurality of arithmetic flags
2 further comprise:

3 a negative data value, a zero data value, a carry out occurrence in a data
4 value, or an overflow condition in a data item in the plurality of data items.

1 10. The method recited in claim 9, wherein the function further comprises:
2 an AND or OR operation.

1 **11.** The method recited in claim 10, wherein the function may be used to
2 determine the status of the plurality of data items, said status comprising:

3 any data item has overflowed;
4 any data item has not overflowed;
5 any data item is positive or zero;
6 any data item is negative;
7 any data item is zero;
8 any data item is not zero;
9 any data item has a carry out;
10 any data item does not have a carry out;
11 all data items have overflowed;
12 all data items have not overflowed;
13 all data items are positive or zero;
14 all data items are negative;
15 all data items are zero;
16 all data items are not zero;
17 all data items have a carry out; and
18 all data items do not have a carry out.

1 **12.** An apparatus comprising a data storage medium for storing
2 instructions when executed by a processor results in, comprising:

3 determining a field size of the plurality of arithmetic flags on which to base a
4 combination process, wherein the plurality of arithmetic flags represent the status of
5 a plurality of data items after a mathematical operation is performed by the
6 processor on the plurality of data items;

7 extracting the plurality of arithmetic flags based on the field size;

8 combining the plurality of arithmetic flags based on a function selected when
9 a combination process is selected; and

10 storing a result of the combining of the plurality of arithmetic flags in a
11 destination register for access by the processor.

1 13. The apparatus recited in claim 12, wherein the field size is based either
2 a nibble, byte, half word, or word in length.

1 14. The apparatus recited in claim 13, wherein the plurality of arithmetic
2 flags further comprise:

3 a negative data value, a zero data value, a carry out occurrence in a data
4 value, or an overflow condition in a data item in the plurality of data items.

1 15. The apparatus recited in claim 14, wherein the function further
2 comprises an AND or OR operation.

1 16. The apparatus recited in claim 15, wherein the function may be used
2 to determine the status of the plurality of data items, said status comprising:

3 any data item has overflowed;
4 any data item has not overflowed;
5 any data item is positive or zero;
6 any data item is negative;
7 any data item is zero;
8 any data item is not zero;
9 any data item has a carry out;
10 any data item does not have a carry out;
11 all data items have overflowed;
12 all data items have not overflowed;
13 all data items are positive or zero;
14 all data items are negative;
15 all data items are zero;
16 all data items are not zero;
17 all data items have a carry out; and
18 all data items do not have a carry out.

1 17. A method of extracting a plurality of arithmetic flags for presentation to
2 a processor, comprising:

3 determining a field size of the plurality of arithmetic flags on which to base a
4 combination process, wherein the plurality of arithmetic flags represent the status of
5 a plurality of data items after a mathematical operation is performed by the
6 processor on the plurality of data items;

7 extracting the plurality of arithmetic flags based on the field size; and
8 storing a result of the extracting of the plurality of arithmetic flags in a
9 destination register for access by the processor.

1 **18.** The method recited in claim 17, wherein the field size is based either
2 a nibble, byte, or half word in length.

1 **19.** The method recited in claim 18, wherein the plurality of arithmetic flags
2 further comprise:

3 a negative data value, a zero data value, a carry out occurrence in a data
4 value, or an overflow condition in a data item in the plurality of data items.

1 **20.** A method of extracting a plurality of arithmetic flags for presentation
2 to a processor, comprising:

3 determining a field size of the plurality of arithmetic flags on which to base a
4 combination process, wherein the plurality of arithmetic flags represent the status of
5 a plurality of data items after a mathematical operation is performed by the
6 processor on the plurality of data items;

7 extracting the plurality of arithmetic flags based on the field size; and
8 storing a result of the extracting of the plurality of arithmetic flags in a
9 destination register for access by the processor.

1 **21.** The method recited in claim 20, wherein the field size is based either
2 a nibble, byte, or half word in length.

1 **22.** The method recited in claim 21, wherein the plurality of arithmetic flags
2 further comprise:

3 a negative data value, a zero data value, a carry out occurrence in a data
4 value, or an overflow condition in a data item in the plurality of data items.